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| **CMPEN 371: Advanced Digital Design** | **Fall 2017** | **Basic Combinational Design** |
|  | **September 27, 2017** |  |

Objectives

* Understand how to design and build a combinational logic circuit in VHDL.
* Learn how to assign the design input and output signals to the target board input/output bins specifically how to wire inputs to the 7-segment channels.
* Learn how to integrate a new logic component with a previously built combinational component in order to come up with new integrated design.

***Learning Instructions:***

* Open Vivado and create new project, name it “Hex2Segment\_display”.

1. Import the Design VHDL file as learned from the previous lab.
2. Import the Constraints Nexys4-DDR file as learned from the previous lab.
3. Choose the Target hardware board.
4. Open the VHDL design file and browse the code to learn the alternative designs found in the same file.
   1. How many designs are found?
   2. Is it sequential or combinational design?
5. Read through the design then modify it so that the decimal point is always ON.
   1. Hint: Use the attached (ModelingConcept) Xilinx tutorial file (*Section 5-2: Model a BCD to 7-Segment Decoder*) to learn the required wiring and input signals of the 7-segment channels available on Nexys4-DDR.
6. Refresh the Design to generate and explore the schematic representation of the design.
7. Synthesize the design and check the outcomes.
8. Implement after synthesizing if no Errors are found.
9. Generate the bit-stream of your design and program the target board if No Errors are found during the implementation stage.
10. Does the connected LEDS work or not? And Why? Can this be fixed and how?

***Lab assignment Exercise:***

1. Use your previous design of 4-bits adder, in addition to modifying this project design code to create a new project where the 4-bits adder’s output is shown on the 7-segment display.
2. In the new project, make all 7-segment channels enabled concurrently, not only a single channel at a time so that the output signal should be repeated (copied) on the eight 7-segment displays.
3. Create a new simulation VHDL file for the project (also known as test bench file).
4. Simulate and check the results for the input values from [0 to 15] (for the first input) and from [9 to 12] for the second input, when the adder’s CarryIn input is set to ZERO. Make sure to include the resulting simulation wave diagrams in your submitted report.
5. Repeat step 4, after setting the CarryIn input to ONE. Make sure to include the resulting simulation wave diagrams in your submitted report.
6. Synthesize the design and check the design report.
7. Implement after synthesizing if no Errors are found.
8. Generate the bit-stream of your design and program the target board if No Errors are found during the implementation stage.

***Deliverables (50 total points)***

1. Complete the lab assignment exercise.
2. Demonstrate your work at the beginning of the next lab period.
3. Take few digital pictures, and short video clip (30 seconds to 1 minute) for your board while it generates the correct output under multiple different input cases (e.g., 5 seconds per case). Embed the Images into the electronic copy of your lab report when submitting. Upload the video to YouTube (as private upload) and include the URL link into your lab report. Name the YouTube video as follows: [CMPEN371\_Fall2017\_BasicCombinationalDesign\_YourTeamSerialCode].
4. Write one lab report per team following the lab guidelines document posted on CANVAS under this lab folder.
   1. Start with the lab report template posted on CANVAS. NOTE: Any text enclosed in braces,{}, is to be replaced or deleted (delete the braces also). Don’t forget to answer the questions at the end of the report.
   2. Turn in one hard copy of the report. The hard copy includes the block diagrams you made while working through the lab.
5. Submit one electronic copy via CANVAS assignments section. Name it BasicCombinationalDesign\_xyz123\_abc456.docx, replacing xyz123 and abc456 with each team members email ID.
   1. Submit all files needed to recreate and test your design, such as all VHDL files, Tcl files, the (.xdc) file, etc. Do not submit the entire Xilinx directory.
6. Deliverables are due at the beginning of your next lab period.